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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DAMIANO, ANNE L	
ART UNIT	**PAPER NUMBER**
2114	5

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/850,112	DOI ET. AL	
	Examiner	Art Unit	
	Anne L Damiano	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7* is/are rejected.

7)☒ Claim(s) *3,6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Allowable Subject Matter

3. Claims 3, 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4, 5 and 7 are rejected under 35 U.S.C. 102(e) as being unpatentable over Edwards et al. (6,684,348).

As in claim 1, Edwards discloses a trace data control circuit (column 1: lines 8-10) comprising:

A branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction (column 8: lines 13-21 and column 6: line 66-column 7: line 11) (When certain watch point triggers occur, such as a branch, trace data is output relating to the branch instruction.)

A CPU-access event generation circuit for outputting a trace data related to a data access instruction (address of an operand accessed in memory) in response to a data access instruction (column 10: lines 34-45 and lines 62-64),

A selection means (MUX) capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events (figure 2: components 203, 204, 205 and 206 and column 8: lines 24-29),

A memory means for storing the trace data (figure 2: component 214, column 2: lines 19-23, column 9: line 65-column 10:line 1), and

A trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data, wherein said branch event generation circuit further comprises an address abbreviation information generation means for detecting an overlapped portion of a branch-source address with a branch-destination address from the upper address bit sides thereof,

and generating a branch-destination address abbreviation information (figure 11A, column 2: lines 41-53, column 4; lines 22-29 and column 18: lines 49-56). (The system has branch watch points. When a branch occurs, the branch information, including the source address and destination address will be output as trace data. The system then compresses the trace data by subtracting a previously sent address from a new address, which is detecting an overlapped portion of addresses. The result is the address offset, which is a branch-destination address abbreviation.)

As in claim 2, Edwards discloses the branch-event generation circuit further comprising:

One or more than one first latching means for latching address data per predetermined number of bits respectively,

One or more than one second latching means for respectively delaying address data for predetermined base clock cycles from the first latching means and latching the delayed data per predetermined number of bits for each (column 4: lines 27-29 and column 8: lines 11-21), (The system can store the previous and new addresses implying that delaying means exist in the system for delaying address data, then latching the delayed data.)

One or more than one comparing means each for comparing the data latched by the first latching means with the data latched by the second latching means per predetermined number of bits and outputting the result of the comparison to the address abbreviation information generation means (column 4: lines 27-29 and column 18: lines 49-54) (Subtracting one address from the other, is comparing the addresses.)

As in claim 4, a trace data control circuit comprising:

A branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction (column 8: lines 13-21 and column 6: line 66-column 7: line 11) (When certain watch point triggers occur, such as a branch, trace data is output relating to the branch instruction.),

A CPU-access event generation circuit for outputting a trace data related to a data access instruction (address of an operand accessed in memory) in response to a data access instruction (column 10: lines 34-45 and lines 62-64),

A selection means capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events (figure 2: components 203, 204, 205 and 206 and column 8: lines 24-29),

A memory means for storing the trace data (figure 2: component 214, column 2: lines 19-23, column 9: line 65-column 10:line 1), and

A trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data,

Wherein the CPU-access event generation circuit further comprises an address abbreviation information generation means for detecting an overlapped portion of a preceding address to be accessed with a succeeding address to be accessed next from the upper address bit sides thereof, in the case of consecutive data access operation, and generating succeeding address abbreviation information (figure 11A, column 2: lines 41-53, column 4; lines 22-29 and column 18: lines 49-56). (The system has an instruction address watch points, when the watch point is

triggered, the address will be output as trace data. The system then compresses the trace data by subtracting a previously sent address from a new address, which is detecting an overlapped portion of addresses. The result is the address offset, which is succeeding address abbreviation information.)

As in claim 5, Edwards discloses the CPU-access event generation circuit further comprising:

One or more than one first latching means for latching address data per predetermined number of bits respectively,

One or more than one second latching means for respectively delaying address data for predetermined base clock cycles from the first latching means and latching the delayed data per predetermined number of bits for each (column 4: lines 27-29 and column 8: lines 11-21), (The system can store the previous and new addresses implying that delaying means exist in the system for delaying address data, then latching the delayed data.)

One or more than one comparing means each for comparing the data latched by the first latching means with the data latched by the second latching means per predetermined number of bits and outputting the result of the comparison to the address abbreviation information generation means (column 4: lines 27-29 and column 18: lines 49-54) (Subtracting one address from the other, is comparing the addresses.)

As in claim 7, Edwards discloses a trace data control circuit comprising:

A branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction (column 8: lines 13-21 and column 6: line 66-column 7: line 11) (When certain watch point triggers occur, such as a branch, trace data is output relating to the branch instruction.),

A CPU-access event generation circuit for outputting a trace data related to a data access instruction (address of an operand accessed in memory) in response to a data access instruction (column 10: lines 34-45 and lines 62-64),

A selection means capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events (figure 2: components 203, 204, 205 and 206 and column 8: lines 24-29),

A memory means for storing the trace data (figure 2: component 214, column 2: lines 19-23, column 9: line 65-column 10:line 1), and

A trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data (column 2: lines 50-58),

Wherein said CPU-access event generation circuit further comprises one or more than one latching means for latching read or write data per predetermined number of bits respectively (column 5: lines 42-48 and column 8: lines 11-21),

One or more than one comparing means each for comparing bit strings held by said one or more than one latching means per predetermined number of bits with a predetermined abbreviation target bit string (column 4: lines 27-29 and column 18: lines 49-54) (Subtracting one address from the other, is comparing the bit strings of the addresses), and

A data abbreviation information generation circuit that inputs the result of the comparison output from said one or more than one comparing means and generates abbreviation information per predetermined number of bits of data related to the read or write data means (column 2: lines 41-53 and column 18: lines 49-54). (The results of the comparing of the previous address with the new address is the abbreviated information a certain number of bits of data relating to the read or write data means.)

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ALD

SCOTT BADERMAN
PRIMARY EXAMINER